B TITLE OF THE INVENTION

Electric or electronic circuit arrangement and method of protecting said circuit arrangement from manipulation and/or abuse

B TECHNICAL FIELD

The present invention relates to an electric or electronic circuit arrangement comprising at least one, particularly layered carrier substrate of a semiconducting or insulating material, at least one integrated circuit constituted by at least two spaced, particularly lithographically applied conductor tracks on the carrier substrate, at least one dielectric shielding layer, particularly an insulation layer and/or passivation layer and/or a further protective layer situated between the conductor tracks and/or laterally with respect to the conductor tracks and/or on the conductor tracks, provided for protecting the integrated circuit from external influences so that the integrated circuit has a specific, particularly lateral and/or particularly parasitic capacitance determined by the dielectric shielding layer.

The invention also relates to a method of protecting an electric or electronic circuit arrangement formed in this way from manipulation and/or abuse.

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In connection with the protection from manipulation and/or abuse, the general trend is that the security requirements, particularly in the field of the smart card chip technique, become more stringent with an increasing use of smart cards such as, for example, bank cards, sickfund cards or various security chip cards. All of these chip cards have in common that sensitive data are stored which should be solely and exclusively accessible to the authorized user of the chip card within the scope defined hereinbefore. In this connection, it is usually the aim of unauthorized persons to read information from the chip card or analyze the functional components of the chip so as to use the chip card for abusive purposes.

A manipulative possibility of obtaining unauthorized information about the structure and/or the function of chip cards is offered by the chemical or mechanical removal of the dielectric shielding layer, particularly the passivation layer, for the purpose of electrical or electronical analysis by means of touching the conductor tracks with (measuring) needles to be put on the conductor tracks and/or for the purpose of optical analysis of the functional components by means of a microscope. In this way, software-defined barriers may be at least partly overcome without authorization. To be able to satisfy the security requirements resulting from these risks of abuse, a concept will be required which combines active and passive security structures such as (photo)sensors and passivation layers.

An arrangement of the type described in the opening paragraph is known from DE 197 38 990 A1. In the arrangement for protecting a chip card from abuse, as described in this document, the dielectrical properties of a passivation layer on the chip of a chip card are scanned by means of a capacitance influenced by the passivation layer. To this end, an oscillator is used whose oscillation frequency is determined by said capacitance. The actual oscillation frequency is compared with a nominal value by clocking a counter in a given time interval and the final count is used as a measure for the actual oscillation frequency.

The number of the count made available by the counter may additionally be combined with a personal, specific number by means of a freely selectable combination algorithm so as to obtain a further number, and the number made available by the counter or the further number may be optionally compared with a reference value.

It is true that this known arrangement implies a number of advantages such as the possibility of preventing abuse due to chip manipulation by means of sensitive capacitance scanning in the capacitance arrangement in the dielectric protective layer shielding the chip, but the envisaged "capacitate sensor" in the arrangement disclosed in DE 197 38 990 A1 is not obtained until after the chip to be protected has been mounted on a card by providing an appropriate protective lacquer and is capable of functioning in this way only.

Based on these drawbacks and shortcomings of the conventional arrangements, it is an object of the present invention to provide an electric or electronic circuit arrangement of the type described in the opening paragraph, as well as a method of protecting an electric or electronic circuit arrangement from manipulation and/or abuse, in which, in contrast to the prior art, a complete integration of the envisaged "capacitive detector" in the (semiconductor) chip is possible without electric connections to the exterior – possibly via contact pads – being required and independent of the fact how the (semiconductor) chip is eventually used. Furthermore, elaborate assembling operations in the actual manufacture of the chip cards are prevented by using the present invention.

This object is solved by the characteristic features defined in claim 1 for an electric or electronic circuit arrangement and by a method, defined in claim 12, of protecting an electric or electronic circuit arrangement from manipulation and/or abuse. Advantageous, further embodiments of the present invention are defined in the dependent claims.

In accordance with the teaching of the present invention, the "capacitive detector", which may also be referred to as "passivation layer sensor", prevents or at least impedes manipulative attacks on an integrated circuit constituted by at least two spaced conductor tracks provided particularly lithographically on a carrier substrate. In this

connection, the concept of the "capacitive detector" or "passivation layer sensor" is based on the use of lateral parasitic capacitances which result from the neighborhood of the at least two conducting, preferably mutually independent conductor tracks.

When the at least one dielectric shielding layer, particularly in the form of at least an insulation layer and/or at least a passivation layer and/or at least a further protective layer, provided for protecting the integrated circuit from external influences, is at least partially removed for manipulative and/or abusive purposes by an unauthorized person, the relative dielectricity value of the insulation layer and/or passivation layer and/or further protective layer situated between the conductor tracks and/or laterally to the conductor tracks and/or on the conductor tracks will be changed. This change $\Delta\varepsilon_r$ of the relative dielectricity value leads to a change ΔC of the specific capacitance in accordance with the formula $\Delta C = \varepsilon_0 \cdot \Delta\varepsilon_r \cdot h \cdot l/d$, in which

- $\varepsilon_0 = 8.8542 \cdot 10^{-12}$ A s V^{-1} m^{-1} is the field constant,
- h is the height of the conductor tracks,
- l is the length of the conductor tracks, and
- d is the distance between the first conductor track and the second conductor track.

When the passivation layer has a relative dielectricity value ε_r of 3.9 or even 7.5 in the case of a shielding silicon nitrite layer, this relative dielectricity value changes after complete removal of the passivation layer to $\varepsilon_{r,Luft} = 1$, i.e. the lateral parasitic capacitances resulting from the neighborhood of the at least two conducting, preferably mutually independent conductor tracks change by a high factor.

The evaluation of this capacitance change may be realized as an absolute measurement or as a relative measurement. When the lateral parasitic capacitance is integrated in an appropriate oscillator circuit such as, for example, an RC oscillator circuit or an LC oscillator circuit, a capacitive sensor can be realized to some extent by evaluating the frequency change resulting from the dielectricity change.

A differential evaluation of the capacitance change described hereinbefore is realized in two steps.

In a first step, the "passivation layer sensor" formed by at least two conductor tracks suitably arranged in parallel and covered by at least one passivation layer is connected to at least one signal-generating unit, particularly to at least one oscillator unit. The capacitance change causes a change of the oscillation frequency.

In a second step, at least two preferably digital counting units are used, in which a first counting unit is clocked at the output frequency of the signal-generating unit,

and a second counting unit is clocked at a reference frequency. When the first counting unit reaches a given predetermined value, the count between the first counting unit and the second counting unit is compared in at least one comparator unit. In the normal case (dielectric shielding layer is neither chemically nor mechanically attacked, or not removed, i.e. the dielectric shielding layer is in good order) the comparison of the count does not lead to an error indication, whereas in the case of manipulation or abuse (dielectric shielding layer is chemically and/or mechanically attacked or removed, i.e. the dielectric shielding layer is out of order) an error indication is generated from the resultant changed frequency.

In summary, it can be concluded that the present invention provides an electric or electronic circuit arrangement as well as a method of protecting an electric or electronic circuit arrangement from manipulation and/or abuse in which – as a delimitation of the arrangement disclosed in DE 197 38 990 A1 – a complete integration of the envisaged "capacitive detector" in the (semiconductor) chip is possible without electric connections to the exterior – possibly via contact pads – being required and independent of the fact how the (semiconductor) chip is eventually used. Furthermore, the present invention precludes elaborate assembling operations in the actual manufacture of the chip cards.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

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In the drawings:

Fig. 1 shows, in a diagrammatical cross-section, an integrated circuit constituted by two spaced conductor tracks provided on a carrier substrate, and

Fig. 2 shows diagrammatically an embodiment of a circuit arrangement in accordance with the present invention.

Identical or similar embodiments, elements or characteristic features are denoted by identical reference signs in Figs. 1 and 2.

B

DETAILED DESCRIPTION

The circuit arrangement 100, shown in Fig. 2, to be implemented and/or integrated in a chip card or smart card comprises a layered carrier substrate 10 of a semiconducting material including processed circuits and conductor tracks up to the penultimate metal plane, as is shown in Fig. 1 in a cross-section. Accordingly, an integrated circuit constituted by two spaced (d) conductor tracks 20, 25 provided lithographically and

arranged sectionally parallel to each other and/or in a meandering intermeshing configuration, in which a first dielectric shielding layer in the form of a passivation layer 30 for protecting the integrated circuit from external influences (cf. Fig. 1) is provided between and laterally to the conductor tracks 20, 25.

A dielectric shielding layer in the form of a further protective layer 35, also for protecting the integrated circuit from external influences, is further provided on the conductor tracks 20, 25, so that the integrated circuit has a specific lateral parasitic capacitance $C = C_{10} + C_{30} + C_{35}$ substantially determined by the two dielectric shielding layers 30, 35 formed from an opaque material (C_{10} is the specific capacitance of the carrier substrate 10).

When one or both dielectric shielding layers in the form of the passivation layer 30 and the further protective layer 35 are at least partially removed, the relative dielectricity value of the dielectric shielding layers situated between the conductor tracks 20, 25, laterally to the conductor tracks 20, 25 and on the conductor tracks 20, 25 changes.

Since the signal-generating unit 40 in the form of an oscillator unit (= oscillator circuit consisting of a capacitive unit, namely a capacitor, and a resistive unit, namely a resistor) is connected to the contact terminals 22 and 27 of the conductor tracks 20 and 25, respectively, in which the output frequency $f_{meas.}$ of this unit is defined by the specific capacitance $C = C_{10} + C_{30} + C_{35}$, the specific capacity change $\Delta C = \varepsilon_0 \cdot \Delta\varepsilon_r \cdot h \cdot l/d$ caused by the change of the relative dielectricity value $\Delta\varepsilon_r$ acts immediately on the output frequency $f_{meas.}$ generated in the signal-generating unit 40.

This signal-generating unit 40 in the form of the RC oscillator unit operates in a reliable manner within a wide voltage and temperature range and at a low current consumption.

The system frequency which is necessary for operating the chip may be utilized as the reference frequency f_{ref}. A further possibility is the use of an additional oscillator having a structure which is similar to that of the oscillator for the measuring frequency, whose frequency-determining elements are, however, accommodated in another insulating layer.

An essential advantage of the signal-generating unit 40 in the form of the RC oscillator unit is the large voltage and temperature range in which the RC oscillator unit operates. When the "capacitive detector", which may also be referred to as "passivation layer sensor", is removed, the oscillation is not interrupted or oscillates at an infinitely large frequency, but is only increased to a multiple of the previous normal frequency.

The signal-generating unit 40 precedes a first digital counting unit 50 clocked at the output frequency $f_{meas.}$ of the signal-generating unit 40 (cf. Fig. 2) in which an actual value count can be determined after a predetermined temporal counting period. The circuit arrangement 100 also comprises a second digital counting unit 55 clocked at a reference frequency f_{ref}, in which a nominal value count can be determined after the predetermined temporal counting period.

In the comparator unit 60, which is preceded by the first counting unit 50 and the second counting unit 55, the actual value count is then compared with the nominal value count, while the functions of the integrated circuit can be blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count (symbol "-" in Fig. 2; when there is no error indication: symbol "+" in Fig. 2), because in this case there is a change of the relative dielectricity value, i.e. a capacitance change, i.e. a frequency shift due to a manipulative and/or abusive attack on the shielding layer dielectric in accordance with the correlations described hereinbefore.

As can also be seen in Fig. 2, a differential evaluation unit 70 is constituted by the first counting unit 50, the second counting unit 55 and the comparator unit 60. This differential evaluation unit 70 is consequently implemented for determining the change of the specific capacitance C caused by an at least partial removal of the dielectric shielding layers 30, 35, which evaluation unit 70 specifically generates the error indication when the actual value deviates from the nominal range.

For a practical realization of the circuit arrangement 100 in accordance with the present invention, it is finally to be noted that the value of the specific capacitance C is dependent on the envisaged oscillator frequency $f_{meas.}$ with the computation of the lateral parasitic capacitance C being based on the equivalent circuit diagram shown in Figs. 1 and 2. For example, it has proved that a lateral capacitance of about $29.7 \cdot 10^{-12}$ F m^{-1} is obtained in the layout when the conductor tracks 20, 25 have a distance d of about two micrometers.

List of reference signs

100	electric or electronic circuit arrangement
10	carrier substrate
20	first conductor track
22	contact terminal of the first conductor track 20
25	second conductor track
27	contact terminal of the second conductor track 25
30	first dielectric shielding layer, particularly passivation layer
35	second dielectric shielding layer, particularly further protective layer
40	signal-generating unit, particularly oscillator unit
50	first counting unit
55	second counting unit
60	comparator unit
70	evaluation unit
C	specific capacitance
ΔC	change of the specific capacitance
C_{10}	specific capacitance of the carrier substrate 10
C_{30}	specific capacitance of the first dielectric shielding layer 30
C_{35}	specific capacitance of the second dielectric shielding layer 35
d	distance between the first conductor track 20 and the second conductor track 25
ε_0	field constant ($\varepsilon_0 = 8.8542 \cdot 10^{-12}$ A s V^{-1} m^{-1})
ε_r	relative dielectricity value
$\Delta\varepsilon_r$	change of the relative dielectricity value
$f_{meas.}$	output frequency of the signal-generating unit 40
f_{ref}	reference frequency
l	length of the conductor tracks 20, 25
$SiNO_2$	silicon nitrite
SiO_2	silicon dioxide